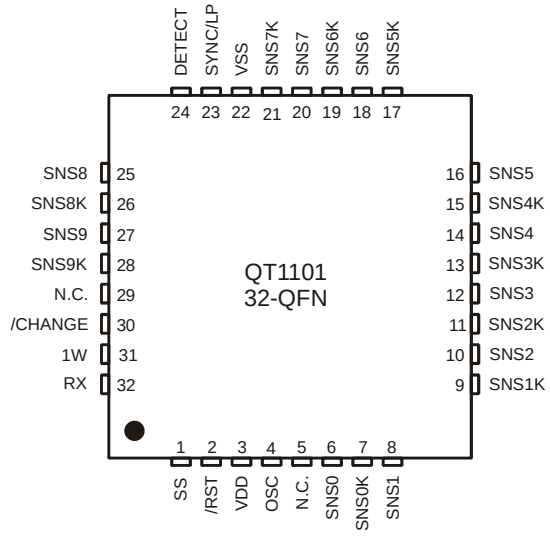
# QT1101

## 10 KEY QTOUCH™ SENSOR IC

- **Patented charge-transfer ('QT') design**
- **Ten independent QT sensing fields (keys)**
- **2.8V ~ 5.5V single supply operation**
- **40µA current typ @ 3V in 360ms LP mode**
- **100% autocal for life - no adjustments required**
- **Serial one or two wire interface with auto baud rate**
- **Fully debounced results**
- **Patented AKS™ Adjacent Key Suppression**
- **Spread spectrum bursts for superior noise rejection**
- **Sync pin for excellent LF noise rejection**
- **'Fast mode' for use in slider type applications**
- **RoHS compliant 32-QFN, 48-SSOP packages**




## APPLICATIONS

- **MP3 players**
- **Mobile phones**
- **PC peripherals**
- **Television controls**
- **Pointing devices**
- **Remote controls**

QT1101 charge-transfer ('QT') QTouch™ IC is a self-contained, patented digital controller capable of detecting near-proximity or touch on up to ten electrodes. It allows electrodes to project independent sense fields through any dielectric such as glass or plastic. This capability coupled with its continuous self-calibration feature can lead to entirely new product concepts, adding high value to product designs. The devices are designed specifically for human interfaces, like control panels, appliances, gaming devices, lighting controls, or anywhere a mechanical switch or button may be found; they may also be used for some material sensing and control applications.

Each of the channels operates independently of the others, and each can be tuned for a unique sensitivity level by simply changing a corresponding external Cs capacitor.

Patented AKS™ Adjacent Key Suppression suppresses touch from weaker responding keys and allows only a dominant key to detect, for example to solve the problem of large fingers on tightly spaced keys.

Spread spectrum burst technology provides superior noise rejection. These devices also have a SYNC/LP pin which allows for synchronization with additional similar parts and/or to an external source to suppress interference, or, an LP (low power) mode which conserves power.

By using the charge transfer principle, this device delivers a level of performance clearly superior to older technologies yet is highly cost-effective.

**AVAILABLE OPTIONS**

| $T_A$ | 32-QFN | 48-SSOP |
|---|---|---|
| -40°C to +85°C | QT1101-ISG | QT1101-IS48G |

# 1 Overview

The QT1101 is an easy to use, ten touch-key sensor IC based on Quantum's patented charge-transfer ('QT') principles for robust operation and ease of design. This device has many advanced features which provide for reliable, trouble-free operation over the life of the product.

**Burst operation:** The device operates in 'burst mode'. Each key is acquired using a burst of charge-transfer sensing pulses whose count varies depending on the value of the reference capacitor Cs and the load capacitance Cx. In LP mode, the device sleeps in an ultra-low current state between bursts to conserve power. The keys signals are acquired using three successive bursts of pulses:

Burst A: Keys 0, 1, 4, 5
Burst B: Keys 2, 3, 6, 7
Burst C: Keys 8, 9

Bursts always operate in A-B-C sequence.

**Self-calibration:** On power-up, all ten keys are self-calibrated within 450ms typical to provide reliable operation under almost any conditions.

**Auto-recalibration**: The device can time out and recalibrate each key independently after a fixed interval of continuous touch detection, so that the keys can never become 'stuck on' due to foreign objects or other sudden influences. After recalibration the key will continue to function normally. The delay is selectable to be either 10s, 60s, or infinite (disabled).

The device also auto-recalibrates a key when its signal reflects a sufficient decrease in capacitance. In this case the device recalibrates after ~2 seconds so as to recover normal operation quickly.

**Drift compensation** operates to correct the reference level of each key slowly but automatically over time, to suppress false detections caused by changes in temperature, humidity, dirt and other environmental effects.

The drift compensation is asymmetric. In the increasing capacitive load direction the device drifts more slowly than in the decreasing direction. In the increasing direction, the rate of compensation is one count of signal per two seconds. In the opposing direction, it is one count every 500ms.

**Detection Integrator (DI) confirmation** reduces the effects of noise on the QT1101 outputs. The DI mechanism requires consecutive detections over a number of measurement bursts for a touch to be confirmed and indicated on the outputs. In a like manner, the end of a touch (loss of signal) has to be confirmed over a number of measurement bursts. This process acts as a type of 'debounce' against noise.

In normal operation, both the start and end of a touch must be confirmed for six measurement bursts. In a special 'Fast Detect' mode (available via jumper resistors) (Tables 1.2 and 1.6), confirmation of the start of a touch requires only two sequential detections, but confirmation of the end of a touch is still six bursts.

Fast detect is only available when AKS is disabled.

**Spread Spectrum operation:** The bursts operate over a spread of frequencies, so that external fields will have minimal effect on key operation and emissions are very weak. Spread spectrum operation works with the DI mechanism to dramatically reduce the probability of false detection due to noise.

**Sync Mode:** The QT1101 features a Sync mode to allow the device to slave to an external signal source, such as a mains signal (50/60Hz), to limit interference effects. This is performed using the SYNC/LP pin. Sync mode operates by triggering three sequential acquire bursts, in sequence A-B-C from the Sync signal. Thus, each Sync pulse causes all ten keys to be acquired.

**Low Power (LP) Mode:** The device features an LP mode for microamp levels of current drain with a slower response time, to allow use in battery operated devices. On detection of touch, the device automatically reverts to its normal mode and asserts the DETECT pin active to wake up a host controller. The device remains in normal, full acquire speed mode until another pulse is seen on its SYNC/LP pin, upon which it goes back to LP mode.

**AKS™ Adjacent Key Suppression** is a patented feature that can be enabled via jumper resistors. AKS works to prevent multiple keys from responding to a single touch, a common complaint about capacitive touch panels. This can happen with closely spaced keys, or with control surfaces that have water films on them.

AKS operates by comparing signal strengths from keys within a group of keys to suppress touch detections from those that have a weaker signal change than the dominant one.

The QT1101 has two different AKS groupings of keys, selectable via option resistors. These groupings are:

AKS operates in three groups of keys.

AKS operates over all ten keys.

These two modes allow the designer to provide AKS while also providing for shift or function operations.

If AKS is disabled, all keys can operate simultaneously.

**Outputs:** The QT1101 has a serial output using one or two wires, RS-232 data format, and automatic baud rate detection. A simple protocol is employed.

The QT1101 operates in slave mode, i.e. it only sends data to the host after receiving a request from the host.

An additional /CHANGE (state changed) signal allows the use of the serial interface to be optimised, rather than being polled continuously.

**Simplified Mode:** To reduce the need for option resistors, the simplified operating mode places the part into fixed settings with only the AKS feature being selectable. LP mode is also possible in this configuration. Simplified mode is suitable for most applications.

## 1.1 Wiring

**Table 1.1 Pinlist**

| 32-QFN Pin | 48 SSOP Pin | Name | Type | Function | Notes | If Unused |
|---|---|---|---|---|---|---|
| 1 | 33 | SS | OD | Spread spectrum | Spread spectrum drive | 100KΩ resistor to Vss |
| - | 34 | n/c | - | - | - | Open |
| 2 | 35 | /RST | I | Reset input | Active low reset | Vdd |
| 3 | 36 | Vdd | Pwr | Power | +2.8 ~ +5.0V | - |
| 4 | 37 | OSC | I | Oscillator | Resistor to Vdd and optional spread spectrum RC network | - |
| 5 | 38 | n/c | - | - | Leave open | - |
| - | 39, 40, 41, 42 | n/c | - | - | - | Open |
| 6 | 43 | SNS0 | I/O | Sense pin and option select | To Cs0 and/or option resistor | Open or option resistor* |
| 7 | 44 | SNS0K | I/O | Sense pin | To Cs0 + Key | Open |
| 8 | 45 | SNS1 | I/O | Sense pin and option select | To Cs1 and/or option resistor* | Open or option resistor* |
| 9 | 46 | SNS1K | I/O | Sense pin | To Cs1 + Key | Open |
| 10 | 47 | SNS2 | I/O | Sense pin and option select | To Cs2 and/or option resistor* | Open or option resistor* |
| 11 | 48 | SNS2K | I/O | Sense pin | To Cs2 + Key | Open |
| 12 | 1 | SNS3 | I/O | Sense pin and option select | To Cs3 and/or option resistor* | Open or option resistor* |
| 13 | 2 | SNS3K | I/O | Sense pin | To Cs3 + Key | Open |
| 14 | 3 | SNS4 | I/O | Sense pin | To Cs4 | Open |
| 15 | 4 | SNS4K | I/O | Sense pin | To Cs4 + Key | Open |
| 16 | 5 | SNS5 | I/O | Sense pin and option select | To Cs5 and/or option resistor * | Open or option resistor* |
| 17 | 6 | SNS5K | I/O | Sense pin | To Cs5 + Key | Open |
| 18 | 7 | SNS6 | I/O | Sense pin and option select | To Cs6 and/or option resistor* | Open or option resistor* |
| 19 | 8 | SNS6K | I/O | Sense pin and mode select | To Cs6 + Key and/or mode resistor† | Open or mode resistor† |
| 20 | 9 | SNS7 | I/O | Sense pin and mode or option select | To Cs7 and/or mode resistor† or option resistor* | Open or mode resistor† or option resistor* |
| 21 | 10 | SNS7K | I/O | Sense pin | To Cs7 + Key | Open |
| - | 11, 12, 13, 14, 15, 16 | n/c | - | - | - | Open |
| 22 | 17 | Vss | Pwr | Ground | 0V | - |
| - | 18, 19, 20 | n/c | - | - | - | Open |
| 23 | 21 | SYNC/LP‡ | I | Sync In or LP In | Rising edge sync or LP pulse | Vdd or Vss** |
| 24 | 22 | DETECT | O/OD | Detect Status | See Table 1.4 | Open |
| - | 23, 24 | n/c | - | - | - | Open |
| 25 | 25 | SNS8 | I/O | Sense pin | To Cs8 | Open |
| 26 | 26 | SNS8K | I/O | Sense pin | To Cs8 + Key | Open |
| 27 | 27 | SNS9 | I/O | Sense pin | To Cs9 | Open |
| 28 | 28 | SNS9K | I/O | Sense pin | To Cs9 + Key | Open |
| 29 | 29 | n/c | - | - | - | Open |
| 30 | 30 | /CHANGE | OD | State changed | 0 = a key state has changed Requires pull-up | 100KΩ resistor to Vss |
| 31 | 31 | 1W | I/OD | 1W mode serial I/O | Requires pull-up to Vdd | - |
| 32 | 32 | RX | I | 2W Receive | Input for 2W mode | Vdd |

**Pin Type**

| | |
|---|---|
| I | CMOS input only |
| I/O | CMOS I/O |
| OD | CMOS open drain output |
| I/OD | CMOS input or open drain output |
| O/OD | CMOS push pull or open-drain output (option selected) |
| Pwr | Power / ground |

**Notes**

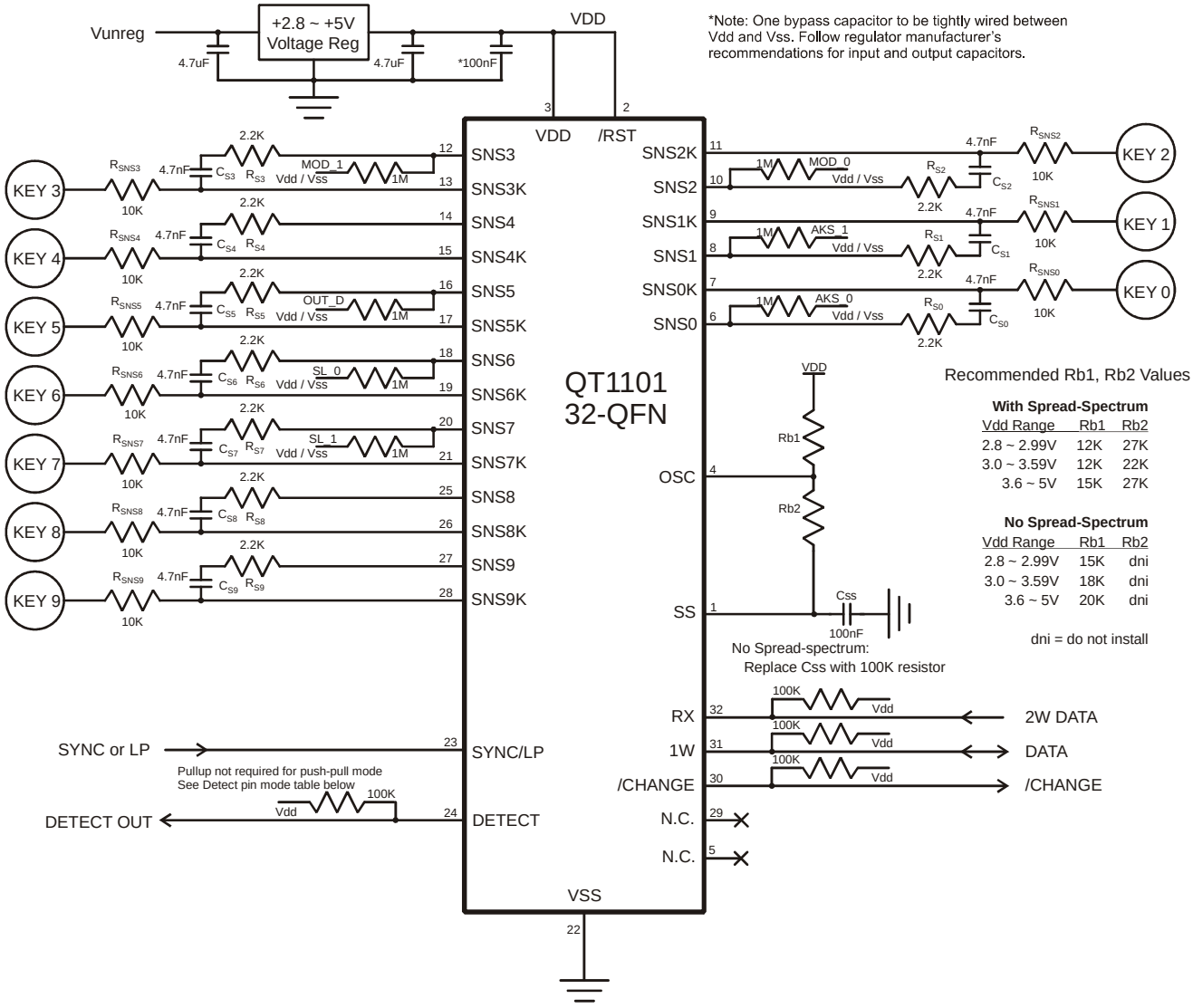
† Mode resistor is required only in Simplified mode (see Figure 1.2)

* Option resistor is required only in Full Options mode (see Figure 1.1)

‡ Pin is either Sync or LP depending on options selected (functions SL_0, SL_1, see Figure 1.1)

** See text

**Figure 1.1 Connection Diagram - Full Options (32-QFN Package)**




Recommended Rb1, Rb2 Values

**With Spread-Spectrum**

| Vdd Range | Rb1 | Rb2 |
|---|---|---|
| 2.8 ~ 2.99V | 12K | 27K |
| 3.0 ~ 3.59V | 12K | 22K |
| 3.6 ~ 5V | 15K | 27K |

**No Spread-Spectrum**

| Vdd Range | Rb1 | Rb2 |
|---|---|---|
| 2.8 ~ 2.99V | 15K | dni |
| 3.0 ~ 3.59V | 18K | dni |
| 3.6 ~ 5V | 20K | dni |

dni = do not install

**Table 1.2**
**AKS / Fast-Detect Options**

| AKS_1 | AKS_0 | AKS MODE | FAST-DETECT |
|---|---|---|---|
| Vss | Vss | Off | Off |
| Vss | Vdd | Off | Enabled |
| Vdd | Vss | On, in 3 groups | Off |
| Vdd | Vdd | On, global | Off |

**Table 1.3**
**Max On-Duration**

| MOD_1 | MOD_0 | MAX ON-DURATION MODE |
|---|---|---|
| Vss | Vss | 10 seconds to recalibrate |
| Vss | Vdd | 60 seconds to recalibrate |
| Vdd | Vss | Infinite (disabled) |
| Vdd | Vdd | (reserved) |

**Table 1.4**
**Detect Pin Drive**

| OUT_D | DETECT PIN MODE |
|---|---|
| Vss | Open drain, active low |
| Vdd | Push-pull, active high |

**Table 1.5**
**SYNC/LP Function**

| SL_1 | SL_0 | SYNC/LP PIN MODE |
|---|---|---|
| Vss | Vss | Sync |
| Vss | Vdd | LP mode: 120ms response time |
| Vdd | Vss | LP mode: 200ms response time |
| Vdd | Vdd | LP mode: 360ms response time |

**Figure 1.2 Connection Diagram - Simplified Mode (32-QFN Package)**

SMR resistor installed between SNS6K, SNS7

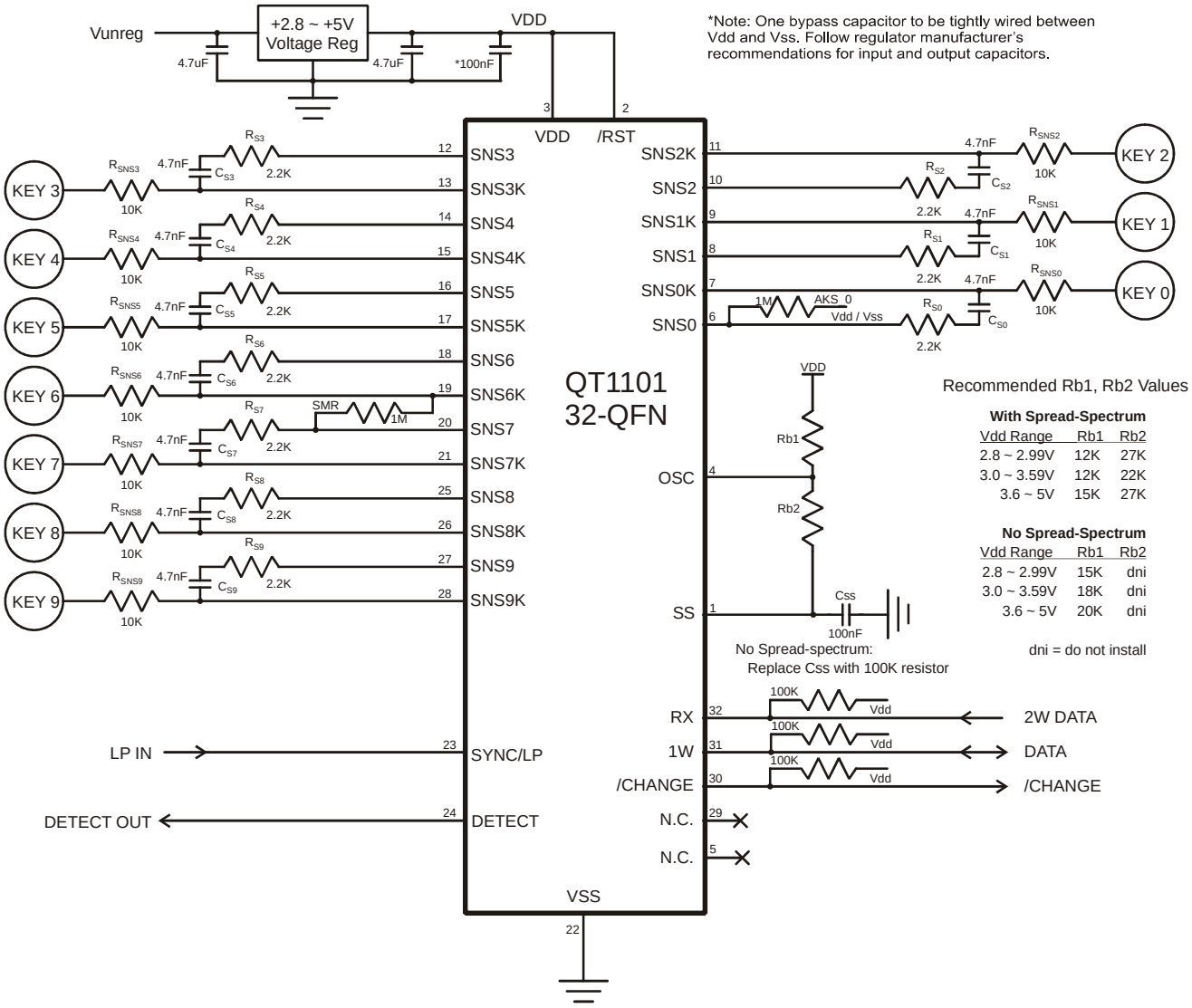



**Table 1.6**
**AKS Resistor Options**

| AKS_0 | AKS MODE | FAST-DETECT |
|---|---|---|
| Vss | Off | Enabled |
| Vdd | On, global | Off |

**Table 1.7**
**Functions in Simplified Mode**

| | |
|---|---|
| **SYNC/LP pin** | 200ms LP function; sync not available |
| **Max on-duration delay** | 60 seconds |
| **Detect Pin** | Push-pull, active high |

# 2 Device Operation

## 2.1 Startup Time

After a reset or power-up event, the device requires 450ms to initialize, calibrate, and start operating normally. Keys will work properly once all keys have been calibrated after reset.

## 2.2 Option Resistors

The option resistors are read on power-up only. There are two primary option mode configurations: full, and simplified.

In full options mode, seven 1MΩ option resistors are required as shown in Figure 1.1. All seven resistors are mandatory.

To obtain simplified mode, a 1MΩ resistor should be connected from SNS6K to SNS7. In simplified mode, only one additional 1MΩ option resistor is required for the AKS feature (Figure 1.2).

Note that the presence and connection of option resistors will influence the required values of Cs; this effect will be especially noticeable if the Cs values are under 22nF. Cs values should be adjusted for optimal sensitivity after the option resistors are connected.

## 2.3 DETECT Pin

DETECT represents the functional logical-OR of all ten keys. DETECT can be used to wake up a battery-operated product upon human touch.

The output polarity and drive of DETECT are governed according to Table 1.4, page 4.

## 2.4 /CHANGE Pin

The /CHANGE pin can be used to tell the host that a change in touch state has been detected (i.e. a key has been touched or released), and that the host should read the new key states over the serial interface. /CHANGE is pulled low when a key state change has occurred.

/CHANGE is very useful to prevent transmissions with duplicate data. If /CHANGE is not used, the host would need to keep polling the QT1101 constantly, even if there are no changes in touch. Upon detection of a key, /CHANGE will pull low and stay low until the serial interface has been polled by the host. /CHANGE will then be released and return high until the next change of key state, either on or off, on any key (Figures 2.1, 2.4).

The /CHANGE pin is open-drain, and requires a ~100K pullup resistor to Vdd in order to function properly.

## 2.5 SYNC/LP Pin

The SYNC / LP pin function is configured according to the SL_0 and SL_1 resistor connections to either Vdd or Vss, according to the Table 1.5.

**Sync mode:** Sync mode allows the designer to synchronize acquire bursts to an external signal source, such as mains frequency (50/60Hz), to suppress interference. It can also be used to synchronize two QT parts which operate near each other, so that they will not cross-interfere if two or more of the keys (or associated wiring) of the two parts are near each other.

The SYNC input is positive pulse triggered. If the SYNC input does not change, the device will free-run at its own rate after ~150ms.

A trigger pulse on SYNC will cause the device to fire three acquire bursts in A-B-C sequence:

Burst A: Keys 0, 1, 4, 5
Burst B: Keys 2, 3, 6, 7
Burst C: Keys 8, 9

**Low Power (LP) Mode:** This allows the device to enter a slow mode with very low power consumption, in one of three response time settings - 120ms, 200ms, and 360ms nominal.

LP mode is entered by a positive pulse on the SYNC/LP pin. Once the LP pulse is detected, the device will enter and remain in this microamp mode until it senses and confirms a touch, upon which it will switch back to normal (full speed) mode on its own, with a response time of <40ms typical (burst length dependent). The device will go back to LP mode again if SYNC/LP is held high or after another LP pulse is received.

The response time setting is determined by option resistors SL_1 and SL_0 (see Table 1.5). Slower response times result in lower power drain.

The SYNC/LP pulse should be >150µs in duration.

If the SYNC/LP pin is held high permanently, the device will go into normal mode during a key touch, and return to low-current mode after the detection has ceased and the key state has been read by the host.

If the SYNC/LP pin is held low constantly, the device will remain in normal full speed mode continuously.

## 2.6 AKS™ Function Pins

The QT1101 features an adjacent key suppression (AKS™) function with two modes. Option resistors act to set this feature according to Tables 1.2 and 1.6. AKS can be disabled, allowing any combination of keys to become active at the same time. When operating, the modes are:

**Global:** The AKS function operates across all ten keys. This means that only one key can be active at any one time.

**Groups:** The AKS function operates among three groups of keys: 0-1-4-5, 2-3-6-7, and 8-9. This means that up to three keys can be active at any one time.

In Group mode, keys in one group have no AKS interaction with keys in any other group.

Note that in Fast Detect mode, AKS can only be off.

## 2.7 MOD_0, MOD_1 Inputs

In full option mode, the MOD_0 and MOD_1 resistors are used to set the 'Max On-Duration' recalibration timeouts. If a key becomes stuck on for a lengthy duration of time, this feature will cause an automatic recalibration event of that specific key only once the specified on-time has been exceeded. Settings of 10s, 60s, and infinite are available.

The Max On-Duration feature operates on a key-by-key basis; when one key is stuck on, its recalibration has no effect on other keys.

The logic combination on the MOD option pins sets the timeout delay; see Table 1.3.

Simplified mode MOD timing: In simplified mode, the max on-duration is fixed at 60 seconds.

## 2.8 Fast Detect Mode

In many applications, it is desirable to sense touch at high speed. Examples include scrolling 'slider' strips or 'Off' buttons. It is possible to place the device into a 'Fast Detect' mode that usually requires under 15 ms to respond. This is accomplished internally by setting the Detect Integrator to only two counts, i.e. only two successive detections are required to detect touch.

In LP mode, 'Fast' detection will not speed up the initial delay (which could be up to 360ms typical depending on the option setting). However, once a key is detected the device is forced back into normal speed mode. It will remain in this faster mode until another LP pulse is received.

When used in a 'slider' application, it is normally desirable to run the keys without AKS.

In both normal and 'Fast' modes, the time required to process a key release is the same: it takes six sequential confirmations of non-detection to turn a key off.

Fast Detect mode can be enabled as shown in Tables 1.2 and 1.6.

## 2.9 Simplified Mode

A simplified operating mode which does not require the majority of option resistors is available. This mode is set by connecting a resistor labeled SMR between pins SNS6K and SNS7. (see Figure 1.2).

In this mode there is only one option available - AKS enable or disable. When AKS is disabled, Fast Detect mode is enabled; when AKS is enabled, Fast Detect mode is off.

AKS in this mode is global only (i.e. operates across all functioning keys).

The other option features are fixed as follows:

**DETECT Pin:** Push-pull, active high

**SYNC/LP Function:** LP mode, ~200ms response time

**Max On-Duration:** 60 seconds

See also Tables 1.6 and 1.7.

## 2.10 Unused Keys

Unused keys should be disabled by removing the corresponding Cs, Rs, and Rsns components and connecting SNS pins as shown in the 'Unused' column of Table 1.1. Unused keys are ignored and do not factor into the AKS function (Section 2.6).

## 2.11 Serial 1W Interface

The 1W serial interface is an RS-232 based auto baud rate serial asynchronous interface that requires only one wire between the host MCU and the QT1101. The serial data are extremely short and simple to interpret.

Auto baud rate detection takes place by having the host device send a specific character to the QT1101, which allows the QT1101 to set its baud rate to match that of the host.

One feature of this method is that the baud rate can be any rate between 8,000 and 38,400 bits per second. Neither the QT1101 nor the host device has to be accurate in their transmission rates, i.e. crystal control is not required.

Depending on the timing of a 1W host transmission, the QT1101 device may need to abort an acquisition burst, and rerun it after the transmission is complete and a reply has been sent. As a consequence, each host request can potentially result in a small, unnoticeable increase in detection delay.

**1W Connection:** The 1W pin should be pulled high with a resistor. When not in use it floats high, hence this causes no increase in supply current.

During transmission from the host, the host may drive the 1W line with either an open-drain or a push-pull driver. However, if the host uses push-pull driving, it must release the 1W line as soon as it is done with its stop bit so that there is no drive conflict when the QT1101 sends its reply.

If open-drain transmission is used by the host, the value of the pull-up resistor should be optimized for the desired baud rate: faster rates require a lower value of resistor to prevent rise-time problems. A typical value for 19,200 baud might be 100KΩ. An oscilloscope should be used to confirm that the resistor is not causing excessive timing skew that might cause bit errors.

The QT1101 uses push-pull drive to transmit data out on the 1W line back to the host. When the stop bit level is established, 1W is floated; for this reason, a pull-up resistor should always be used on the 1W pin to prevent the signal from drifting to an undefined state. A 100KΩ pull-up resistor on 1W is recommended, unless the host uses open-drain drive to the QT1101, in which case a lower value may be required (see prior paragraph).

### 2.11.1 Basic 1W Operation

The basic sequence of 1W serial operation is shown in Figure 2.1. The 1W line is bi-directional and must be pulled high with a resistor to prevent a floating, undefined state (see previous section).

**Figure 2.1 Basic 1W Sequence**

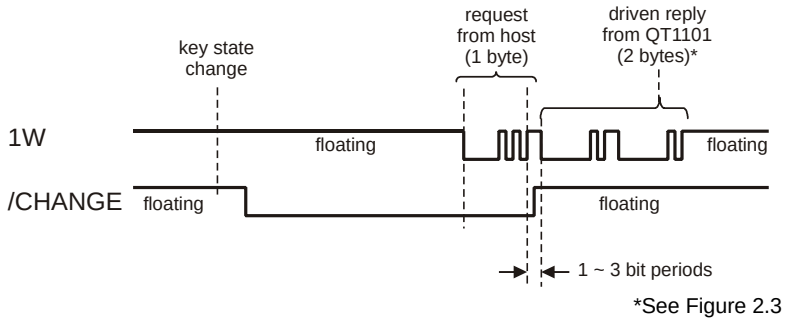
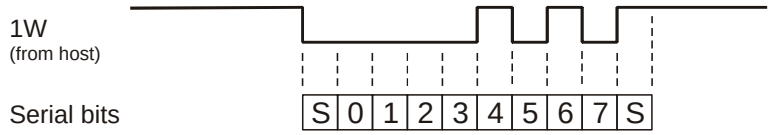
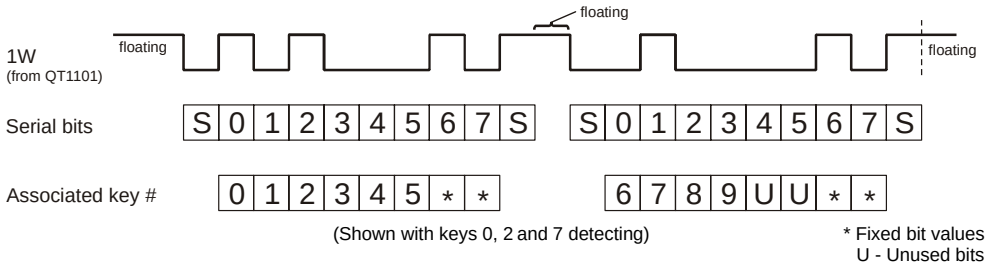



**Figure 2.2 1W UART Host Pattern**



**Oscillator Tolerance:** While the auto baud rate detection mechanism has a wide tolerance for oscillator error, the QT's oscillator should still not vary by more than ±20% from the recommended value. Beyond a 20% error, communications at either the lower or upper stated limits could fail. The oscillator frequency can be checked with an oscilloscope by probing the pulse width on the SNS lines; these should ideally be 2.15µs in width each at the beginning of a burst with the recommended spread-spectrum circuit, or 2µs wide if no spread-spectrum circuit is used.

**Figure 2.3 UART Response Pattern on 1W Pin**




**Host Request Byte:** The host requests the key state from the QT1101 by sending an ASCII "P" character (ASCII decimal code 80, hex 0x50) over the 1W line. The character is formatted according to conventional RS-232:

8 data bits
no parity
1 stop bit
baud rate: 8,000 - 38,400

Figure 2.2 shows the bit pattern of the host request byte ('P'). The first bit labeled 'S' is the start bit, the last 'S' is the stop bit. This bit pattern should never be changed. The QT1101 will respond at the same baud rate as the received 'P' character.

After sending the 'P' character the host must immediately float the 1W signal to prevent a drive conflict between the host and the QT1101 (see Figure 2.1). The delay from the received stop bit to the QT1101 driving the 1W pin is in the range 1-3 bit periods, so the host should float the pin within one bit period to prevent a drive conflict.

**Data Reply:** Before sending a reply, the QT1101 returns the /CHANGE signal to its inactive (float-high) state.

The QT1101 then replies by sending two eight-bit characters to the host over the 1W line using the same baud rate as the request. With no keys pressed, both repl y bytes are ASCII '@' (0x40) characters; any keys that are pressed at the time of the reply result in their associated bits being set in the reply. Figure 2.3 shows the reply bytes when keys 0, 2 and 7 are pressed - 0x45, 0x42, and the associations between keys and bits in the reply.

The QT1101 floats the 1W pin again after establishing the level of the stop bit.

### 2.11.2 LP Mode Effects on 1W

The use of low power (LP) mode presents some additional 1W timing requirements. In LP mode (Section 2.5), the QT1101 will only respond to a request from the host when it is making one of its infrequent checks for a key press. Hence, in that condition most requests from the host to the QT1101 will be ignored, since the QT1101 will be sleeping and unresponsive. However, if either /CHANGE or DETECT are active the QT1101 will be at full speed, and hence will always respond to 'P' requests.

Note that when sleeping in LP mode, there are by definition no keys active, so there should not be a reason for the host to send the 'P' query command in the first place.

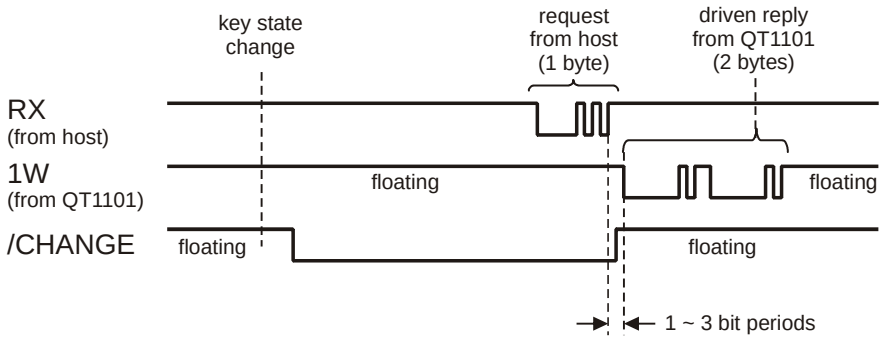
Three strategies are available to the host to ensure that LP mode operates correctly:

- **/CHANGE used**. The host monitors /CHANGE, and only sends a 'P' request when it is low. The part is awake by definition when /CHANGE is low. If /CHANGE is high, key states are known to be unchanged since the last reply received from the QT1101, and so additional 'P' requests are not needed. Before triggering LP mode the host should wait for /CHANGE to go high after all keys have become inactive.
- **DETECT used**. The host monitors DETECT, and if it is active (i.e. the part is awake) it polls the device regularly to obtain key status. When DETECT is inactive (the part may be sleeping) no requests are sent because it is known that no keys are active. Before triggering LP mode the host should wait for DETECT to become inactive, and then send one additional 'P' request to ensure /CHANGE is also made inactive.
- **Neither /CHANGE nor DETECT used**. The host polls the device regularly to obtain key status, with a timeout in operation when awaiting the reply to each 'P' request. Not receiving a reply within the timeout period only occurs when the part is sleeping, and hence when no keys are active. Before triggering LP mode the host should wait for all keys to become inactive and then send an additional 'P' request to the QT1101 to ensure /CHANGE is also inactive.

### 2.11.3 2W Operation

1W operation, as described above, requires that the host float the 1W line while awaiting a reply from the QT1101; this is not always possible.

**Figure 2.4 2W Operation**



To solve this problem, the QT1101 can also receive the 'P' character from the host on its 'Rx' pin separately from the 1W pin (Figure 2.4). The host need not float the Rx line since the QT1101 will never try to drive it.

Following a 'P' on Rx, the QT1101 will send the same response pattern (Figure 2.3) over the 1W line as in pure 1W mode.

All other comments and timings given for 1W operation are applicable for 2W operation. LP operation is the same for 2W mode as for 1W.

If the Rx pin is not used, it must be tied to Vdd.

# 3 Design Notes

## 3.1 Oscillator Frequency

The QT1101's internal oscillator runs from an external network connected to the OSC and SS pins as shown in Figures 1.1 and 1.2. The charts in these figures show the recommended values to use depending on nominal operating voltage and spread spectrum mode.

If spread spectrum mode is not used, only resistor Rb1 should be used, the Css capacitor eliminated, and the SS pin pulled to Vss with a 100K resistor.

An out-of-spec oscillator can induce timing problems such as large variations in Max On-Duration times and response times as well as on the serial port.

**Effect on serial communications:** The oscillator frequency has no nominal effect on serial communications since the baud rate is set by an auto-sensing mechanism. However, if the oscillator is too far outside the recommended settings, the possible range of serial communications can shrink. For example, if the oscillator is too slow, the upper baud rate range can be reduced.

The burst pulses should always be in the range of 1.8-2.4µs at the start of a burst to allow the serial port to operate at its specified limits; in spread-spectrum mode, the first pulses of a burst should ideally be 2.15µs. In non spread-spectrum mode, the target value is 2µs. If in doubt, make the pulses on the narrower side (i.e. a faster oscillator) when using the higher baud rates, and conversely on the wider side when using the lowest baud rates.

## 3.2 Spread Spectrum Circuit

The QT1101 offers the ability to spectrally spread its frequency of operation to heavily reduce susceptibility to external noise sources and to limit RF emissions. The SS pin is used to modulate an external passive RC network that modulates the OSC pin. OSC is the main oscillator current input. The circuits and recommended values are shown in Figures 1.1 and 1.2.

The resistors Rb1 and Rb2 should be changed depending on Vdd. As shown in Figures 1.1 and 1.2, three sets of values are recommended for these resistors depending on Vdd. The power curves in Section 4.6 also show the effect of these resistors.

The spread-spectrum circuit can be eliminated if it is not desired (see Section 3.1). Non spread-spectrum mode consumes significantly less current in one of the LP modes.

The spread-spectrum RC network might need to be modified slightly with longer burst lengths. The sawtooth waveform observed on SS should reach a crest height as follows:

Vdd >= 3.6V: 17% of Vdd
Vdd < 3.6V: 20% of Vdd

The Css capacitor connected to SS (Figures 1.1 and 1.2) should be adjusted so that the waveform approximates the above amplitude, ±10%, during normal operation in the target circuit. If this is done, the circuit will give a spectral modulation of 12-15%.

## 3.3 Cs Sample Capacitors - Sensitivity

The Cs sample capacitors accumulate the charge from the key electrodes and determine sensitivity. Higher values of Cs make the corresponding sensing channel more sensitive. The values of Cs can differ for each channel, permitting differences in sensitivity from key to key or to balance unequal sensitivities. Unequal sensitivities can occur due to key size and placement differences and stray wiring capacitances. More stray capacitance on a sense trace will desensitize the corresponding key; increasing the Cs for that key will compensate for the loss of sensitivity.

The Cs capacitors can be virtually any plastic film or low to medium-K ceramic capacitor. The 'normal' Cs range is 2.2nF to 50nF depending on the sensitivity required; larger values of Cs require better quality to ensure reliable sensing. Acceptable capacitor types for most uses include PPS film, polypropylene film, and NP0 and X7R ceramics. Lower grades than X7R are not advised.

The required values of Cs can be noticeably affected by the presence and connection of the option resistors.

## 3.4 Power Supply

The power supply can range from 2.8V to 5.0V. If this fluctuates slowly with temperature, the device will track and compensate for these changes automatically with only minor changes in sensitivity. If the supply voltage drifts or shifts quickly, the drift compensation mechanism will not be able to keep up, causing sensitivity anomalies or false detections.

The power supply should be locally regulated using a three-terminal device, to between 2.8V and 5.0V. If the supply is shared with another electronic system, care should be taken to ensure that the supply is free of digital spikes, sags, and surges which can cause adverse effects.

For proper operation a 0.1µF or greater bypass capacitor must be used between Vdd and Vss. The bypass capacitor should be routed with very short tracks to the device's Vss and Vdd pins.

## 3.5 PCB Layout and Construction

Refer to Quantum application note AN-KD02 for information related to layout and construction matters.

# 4 Specifications

## 4.1 Absolute Maximum Specifications

Operating temperature, Ta. . . . . -40 ~ +85ºC
Storage temp, Ts. . . . . -50 ~ +125ºC
Vdd. . . . . -0.3 ~ +6.0V
Max continuous pin current, any control or drive pin. . . . . ±20mA
Short circuit duration to ground or Vdd, any pin. . . . . infinite
Voltage forced onto any pin. . . . . -0.3V ~ (Vdd + 0.3) Volts

## 4.2 Recommended Operating Conditions

Operating temperature, Ta. . . . . -40 ~ +85ºC
$V_{DD}$. . . . . +2.8 ~ +5.0V
Short-term supply ripple+noise. . . . . ±5mV/s
Long-term supply stability. . . . . ±100mV
Cs range. . . . . 2.2 ~ 100nF
Cx range. . . . . 0 ~ 50pF

## 4.3 AC Specifications

Vdd = 5.0V, Ta = recommended, Cx = 5pF, Cs = 4.7nF; circuit of Figure 1.1

| Parameter | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Trc | Recalibration time | | 300 | | ms | |
| Fc | Burst center frequency | | 124 | | kHz | |
| Fm | Burst modulation, percent | | 15 | | % | Total deviation |
| Tpc | Sample pulse duration | | 2 | | µs | |
| Tsu | Startup time from cold start | | 450 | | ms | |
| Tbd | Burst duration | | 6.5 | | ms | All 3 bursts |
| Tdf | Response time - Fast mode | | 15 | | ms | |
| Tdn | Response time - normal mode | | 40 | | ms | |
| Tdl | Response time - LP mode | | 200 | | ms | 200ms LP setting |
| Tdr | Release time - all modes | | 40 | | ms | End of touch |
| bps | Serial communications speed | 8,000 | | 38,400 | baud | |

## 4.4 DC Specifications

Vdd = 5.0V, Ta = recommended, Cx = 5pF, Cs = 4.7nF, Ta = recommended range; circuit of Figure 1.1 unless noted

| Parameter | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Iddn | Average supply current, normal mode* | | 4.5<br>2.7<br>2.1<br>1.9<br>1.5 | 8 | mA | @ Vdd = 5.0<br>@ Vdd = 4.0<br>@ Vdd = 3.6<br>@ Vdd = 3.3<br>@ Vdd = 2.8 |
| Iddl | Average supply current, LP mode* | | 75 | | µA | @ Vdd = 3.0; 200ms LP mode |
| Vdds | Average supply turn-on slope | 100 | | | V/s | Req'd for startup, w/o external reset ckt |
| Vil | Low input logic level | | | 0.7 | V | |
| Vhl | High input logic level | 3.5 | | | V | |
| Vol | Low output voltage | | | 0.5 | V | 7mA sink |
| Voh | High output voltage | Vdd-0.5 | | | V | 2.5mA source |
| Iil | Input leakage current | | | ±1 | µA | |
| Ar | Acquisition resolution | | 8 | | bits | |

***No spread spectrum circuit**

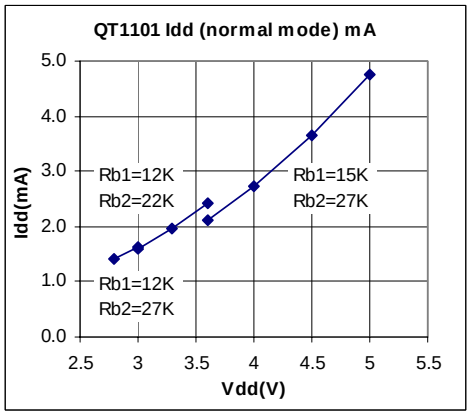
## 4.5 Signal Processing

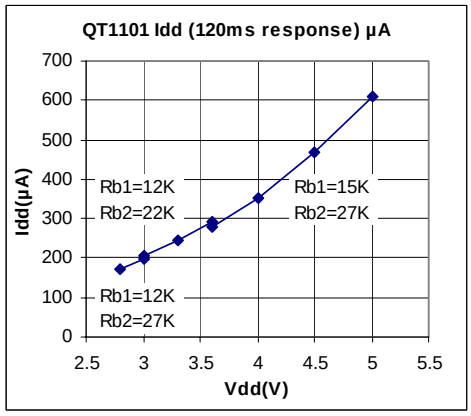
Vdd = 5.0V, Ta = recommended, Cx = 5pF, Cs = 4.7nF, 2µs QT Pulses

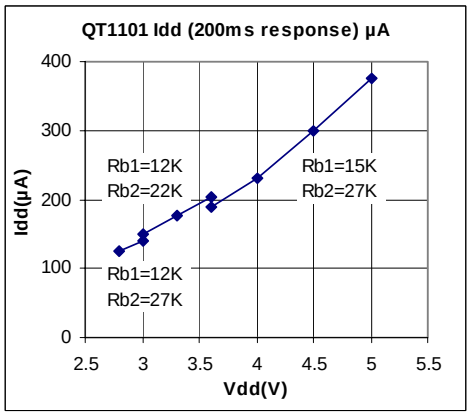
| Description | Value | Units | Notes |
|---|---|---|---|
| Detection threshold | 10 | counts | Threshold for increase in Cx load |
| Detection hysteresis | 2 | counts | |
| Anti-detection threshold | 6 | counts | Threshold for decrease of Cx load |
| Anti-detection recalibration delay | 2 | secs | Time to recalibrate if Cx load has exceeded anti-detection threshold |
| Detect Integrator filter, normal mode | 6 | samples | Must be consecutive or detection fails |
| Detect Integrator filter, Fast mode | 2 | samples | Must be consecutive or detection fails |
| Max On-Duration | 10, 60, inf | secs | Option pin selected |
| Normal drift compensation rate | 2,000 | ms/level | Towards increasing Cx load |
| Anti drift compensation rate | 500 | ms/level | Towards decreasing Cx load |

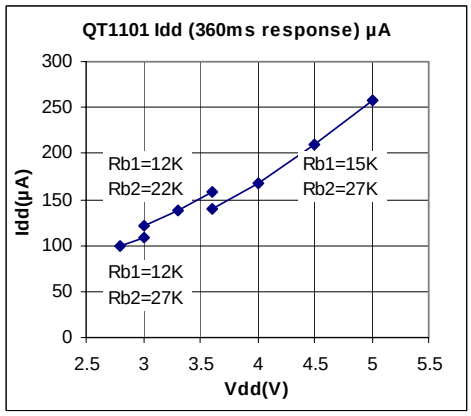
## 4.6 Idd Curves

Cx = 5pF, Cs = 4.7nF, Ta = 20°C, Spread spectrum circuit (see Fig. 1.1).

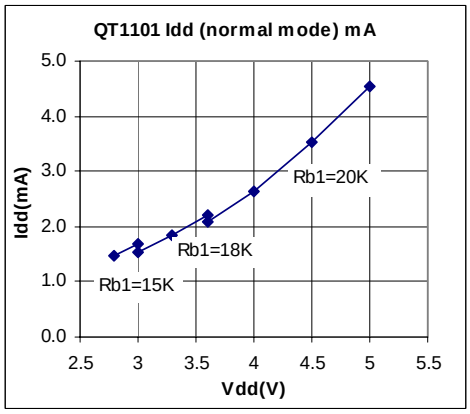


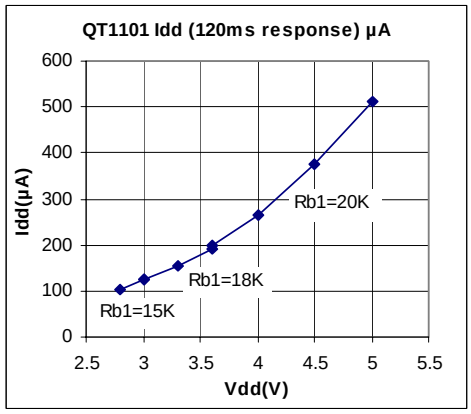



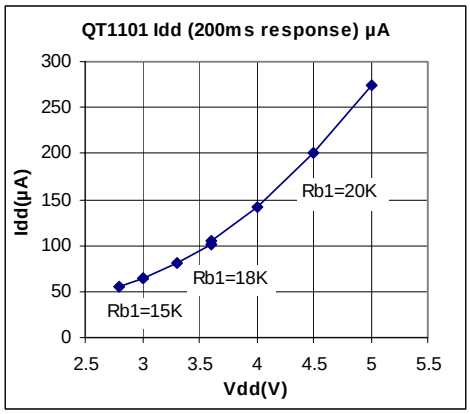



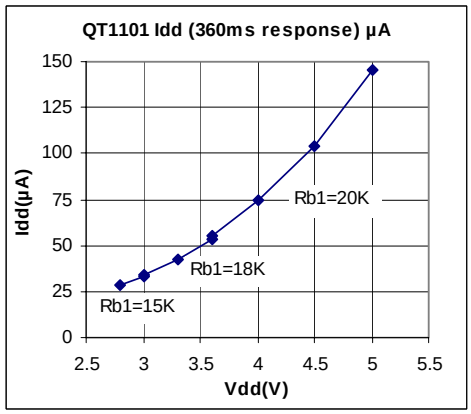




Cx = 5pF, Cs = 4.7nF, Ta = 20°C, No spread spectrum circuit (see Fig. 1.1).

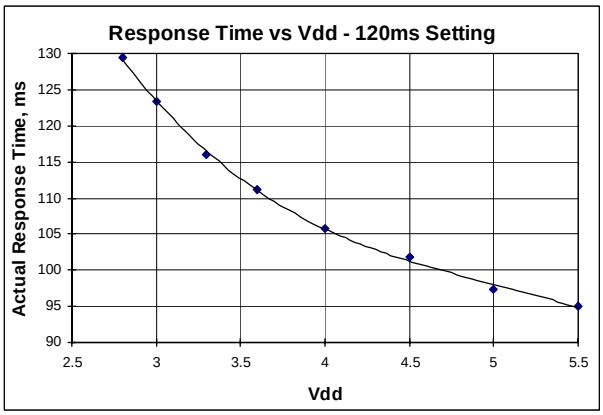


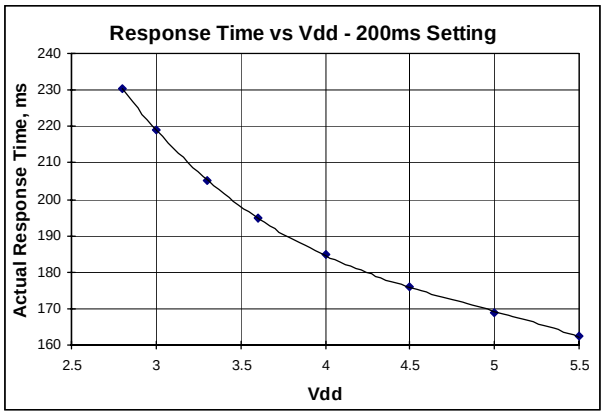



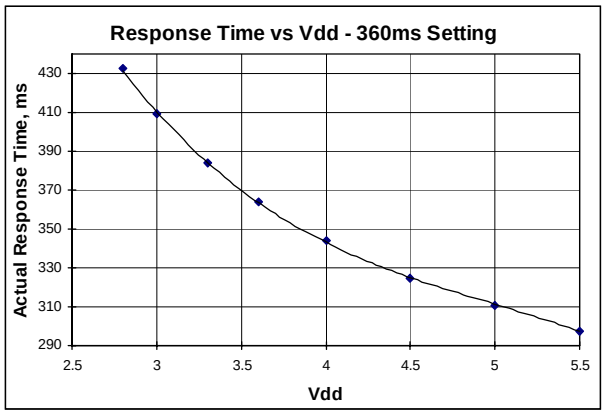



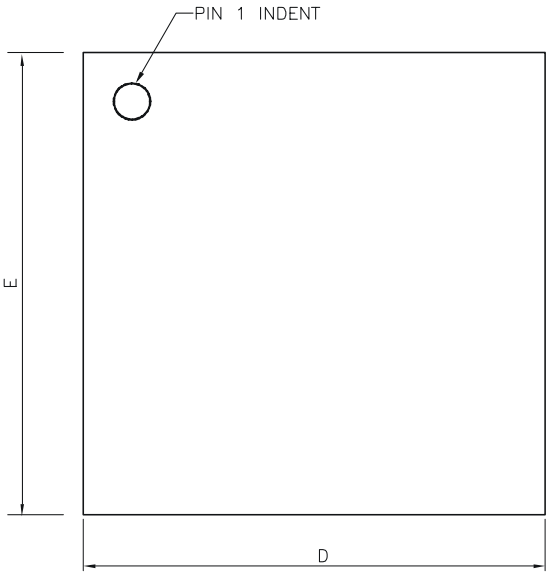
## 4.7 LP Mode Typical Response Times

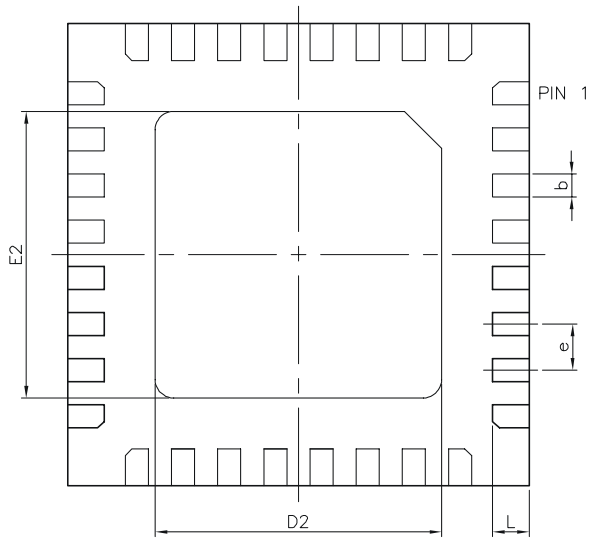


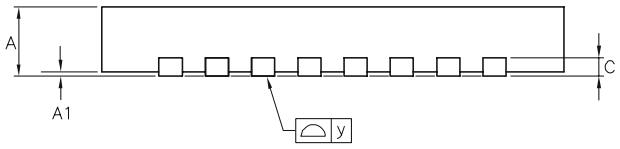



## 4.8 Mechanical - 32-QFN Package



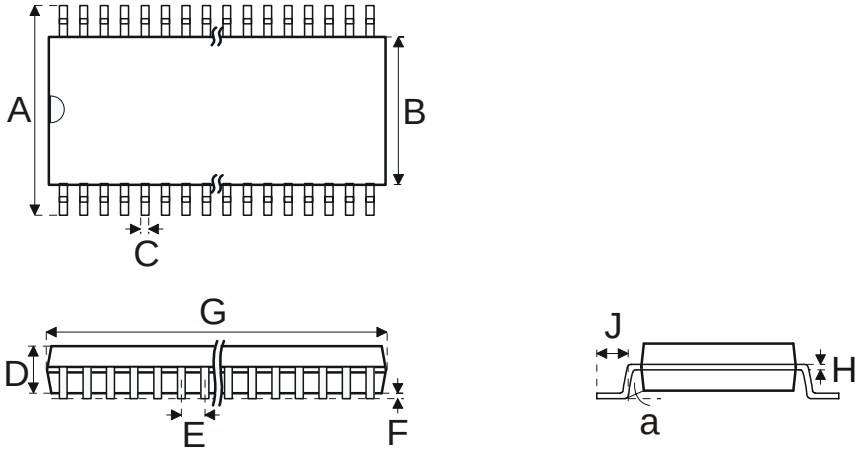




| Dimensions In Millimeters | | | |
|---|---|---|---|
| **Symbol** | **Minimum** | **Nominal** | **Maximum** |
| A | 0.70 | - | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.32 |
| C | - | 0.20 REF | - |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.05 | - | 3.65 |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.05 | - | 3.65 |
| e | - | 0.50 | - |
| L | 0.30 | 0.40 | 0.50 |
| y | 0.00 | - | 0.075 |

Note that there is no functional requirement for the large pad on the underside of the 32-QFN package to be soldered to the substrate. If the final application does require this area to be soldered for mechanical reasons, the pad(s) to which it is soldered to must be isolated and contained under the 32-QFN footprint only.

## 4.9 Mechanical - 48-SSOP Package

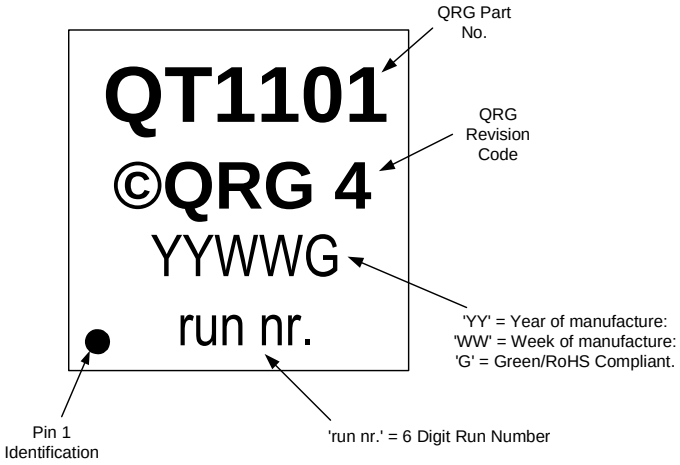



All dimensions in millimeters

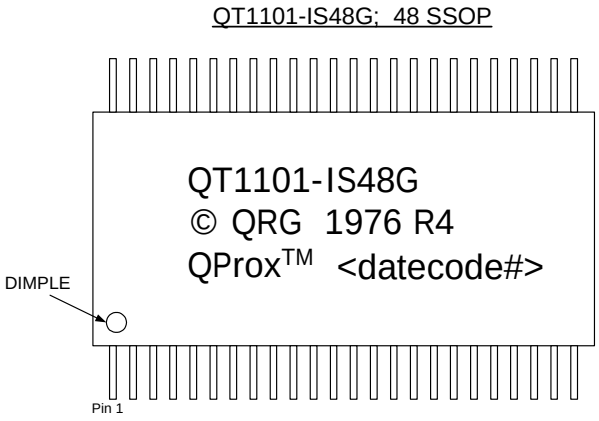
| | A | B | C | D | E | F | G | H | J | a |
|---|---|---|---|---|---|---|---|---|---|---|
| **Min** | 10.03 | 7.39 | 0.20 | 2.16 | 0.64 Typ | 0.10 | 15.57 | 0.10 | 0.64 | 0° |
| **Max** | 10.67 | 7.59 | 0.30 | 2.51 | | 0.25 | 16.18 | 0.30 | 0.89 | 8° |

## 4.10 Part Marking

**32-QFN**




**48-SSOP**



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